REMARKS

In response to the Office Action mailed August 31, 2004, Applicant respectfully requests reconsideration. To further the prosecution of this Application, Applicant submits the following remarks and has added new claims. The claims as now presented are believed to be in allowable condition.

Claims 1-22 were pending in this Application. Claims 23-30 have been added. Accordingly, claims 1-30 are now pending in this Application. Claims 1, 8, 15 and 22 are independent claims.

Objection to the Specification

The Office Action objected to the Specification contending that the Title is not descriptive. In order to further the prosecution of this Application, Applicant has replaced the original Title with a new Title. Applicant submits that this new Title is descriptive. Accordingly, the objection to the Specification should be withdrawn.

Objection to the Drawings

The Office Action objected to the drawings contending that certain reference characters were not mentioned in the description. Applicant has amended the Specification to correct these informalities. No new matter has been added. Accordingly, the objection to the Drawings should be withdrawn.

Objection to Claim 15

The Office Action objected to claim 15 due to a minor informality. Applicant has made a minor clarifying amendment to claim 15 to cure this minor informality. Applicant was careful not to raise any new issues that would require further searching and/or consideration by the Patent Office. Accordingly, the objection to claim 15 should be withdrawn.

Applicant wishes to point out that Applicant has also made a minor clarifying amendment to claim 17 for consistency.

Rejections under §102 and §103

Claims 1, 4-5 and 7 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,237,077 (Sharangpani et al.). Claim 2 was rejected under 35 U.S.C. §103(a) as being unpatentable over Sharangpani et al. in view of Hennessy and Patterson, Computer Architecture – A Quantitative Approach, 2nd Edition, 1996 (Hennessey). Claim 3 was rejected under 35 U.S.C. §103(a) as being unpatentable over Sharangpani et al. in view of U.S. Patent No. 5,748,978 (Narayan et al.). Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over Sharangpani et al. in view of U.S. Patent No. 6,233,671 (Abdallah et al.). Claims 8, 11-12, 14-15, 18-19 and 21-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of U.S. Patent No. 5,278,974 (Lemmon et al.) in further view of Sharangpani et al. Claims 9 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Lemmon in view of Sharangpani et al., and in further view of Hennessey. Claims 10 and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Lemmon in view of Sharangpani et al., and in further view of Narayan et al. Claims 13 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Lemmon in view of Sharangpani et al., and in further view of Abdallah et al.

Applicant respectfully traverses each of these rejections and requests reconsideration. The claims are in allowable condition.

Sharangpani discloses a microprocessor architecture for processing branch instructions (column 1, lines 4-9). Such an architecture simplifies the logic necessary to process branch instructions and facilitates suppression of issued instructions following a taken branch (column 2, lines 65-67). Along these lines, a template field 220 encodes a template type that indicates how instruction slots 210 are mapped to execution units (column 4, lines 64-67). That is, Sharangpani discloses a pipeline 300 having an instruction buffer stage 302 and a dispersal stage 304 (column 6, lines 42-44 and Fig. 3). The instruction buffer stage 302 includes an instruction buffer 320 for receiving instruction bundles 200,

and dispersal stage 304 includes a dispersal network 340 for routing instructions from instruction buffer 320 to execution units in a subsequent stage of the pipeline 300 (column 6, lines 45-49). In one embodiment, the buffer 320 may be an instruction cache (column 7, lines 12-13).

Applicant's Admitted Prior Art (AAPA) discloses a conventional data storage system having memory circuit boards which are configured to respond to a small set of basic instructions such as READ, WRITE, ADD and MASK-COMPARE-AND-SWAP commands (page 2, lines 5-7). Unfortunately, communications between interfaces and the memory circuit boards of the data storage system require several separate communications (page 2, lines 24-25). The large number of communications results in poor response time due to delays, e.g., handshaking delays in waiting for a memory circuit board to complete an operation incrementally before sending a communication for a next operation, resource contention delays due to contention for a bus or buses, etc. (page 3, lines 3-8).

Claims 1-7

Claim 1 is directed to a method which is performed in a memory circuit board that stores a cache for a data storage system. The method includes the step of receiving a communication that includes a script command and a payload. The payload includes a series of individual instructions. The method further includes the step of parsing the payload to identify the series of individual instructions in response to the script command. The method further includes the step of performing a series of operations in accordance with the identified series of individual instructions.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art

reference."[1] "The identical invention must be shown in as complete detail as is contained in the ... claim."[2] In Sharangpani, there is no disclosure of a method, which is performed in a memory circuit board that stores a cache for a data storage system, having a step of performing a series of operations in accordance with an identified series of individual instructions parsed from a payload of a communication having both a script command and the payload, as recited in claim 1. Rather, Sharangpani discloses a microprocessor architecture for routing instructions from an instruction buffer 320 to execution units in a subsequent stage of a pipeline 300 (e.g., see column 6, lines 42-49 and Fig. 3 of Sharangpani).

The Office Action, in paragraph 7, contends that Sharangpani discloses a script command 220 and a payload 210a-c having series of individual instructions, i.e., three instructions 210a, 210b, 210c. The Office Action, paragraph 7, further contends that Sharangpani discloses performing a series of operations in accordance with the identified series of individual instructions 210a, 210b, 210c. Applicant respectfully traverses this contention. Sharangpani does not disclose performing a series of operations in accordance with a series of individual instructions 210a, 210b, 210c. To the contrary, Sharangpani discloses routing the instructions 210a, 210b, 210c from an instruction buffer 320 to different execution units (e.g., see column 4, lines 64-67 of Sharangpani).

Moreover, it is unclear how one could modify Sharangpani to perform a series of operations in accordance with the identified series of individual instructions 210a, 210b, 210c since a major point of Sharangpani seems to be to routing instructions to different execution units. Nothing in the other cited references teach or suggest how one could modify Sharangpani along these lines.

---

[1] *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

[2] *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

For the reasons stated above, claim 1 patentably distinguishes over the cited prior art, and the rejection of claim 1 under 35 U.S.C. §102(e) should be withdrawn. Accordingly, claim 1 is in allowable condition.

Because claims 2-7 depend from and further limit claim 1, claims 2-7 are in allowable condition for at least the same reasons.

Claims 8-14

Claim 8 is directed to a data storage system which includes (a) a set of storage devices; (b) a memory circuit board that stores a cache to temporarily store copies of data elements stored in the set of storage devices; and (c) a processor circuit board that operates as at least one of a front-end interface between an external device and the cache and a back-end interface between the cache and the set of storage devices. The memory circuit board is configured to (i) receive, from the processor circuit board, a communication that includes a script command and a payload, the payload including a series of individual instructions, (ii) parse the payload to identify the series of individual instructions in response to the script command, and (iii) perform a series of operations in accordance with the identified series of individual instructions.

The cited prior art does not teach or suggest, either alone or in combination, a data storage system having a memory circuit board configured to (i) receive, from the processor circuit board, a communication that includes a script command and a payload, the payload including a series of individual instructions, (ii) parse the payload to identify the series of individual instructions in response to the script command, and (iii) perform a series of operations in accordance with the identified series of individual instructions, as recited in claim 8. The Office Action in paragraph 19 even submits that the AAPA teaches sending instructions, one at a time, to a memory circuit board and that the AAPA does not teach packing multiple instructions together and transmitting them to a memory circuit board at a single time. Applicants agree.

However, the Office Action then contends that teaches that (i) some amount of overhead is required for every data transfer, as taught by Lemmon, (ii) if a packet is able to hold three instructions, then only two transfers will need to be made, resulting in four less time units required to perform the transfer, and (iii) in view of the amount of transfer time being reduced, it would have been obvious to one of ordinary skill in the art to modify the AAPA to package multiple instructions and transfer them together. Applicant respectfully disagrees. This contention is not only incorrect, it applies the incorrect test for obviousness under 35 U.S.C. §103(a).

In order to establish a *prima facie* case of obviousness, the Office Action must meet three criteria.

> "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."[3]

If one applies the correct test, it will be clear that the AAPA and Lemmon do not teach or suggest all of the claim limitation. Specifically, neither reference teaches or suggests a memory circuit board configured to perform a series of operations in accordance with an identified series of individual instructions parsed from a payload of a communication having both a script command and the payload, as recited in claim 8.

In an attempt to add such a teaching, the Office Action then contends that Sharangpani teaches that an instruction packet includes a script command and a payload, the payload including a series of individual instructions (see the first sentence at the top of page 10 of the Office Action). This contention is wrong. Sharangpani does not teach the use of packets. Furthermore, Sharangpani does not teach the use of instructions within a memory circuit board of a data storage

---

[3] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

system. As explained above in connection with claim 1, Sharangpani teaches routing instructions to different execution units within a microprocessor architecture. Accordingly, the cited prior art does not teach or suggest all of the claim limitations. Additionally, the cited prior art does not provide any suggestion or motivation to modify the reference or to combine reference teachings. Moreover, the cited prior art does not provide any reasonable expectation of success.

For the reasons stated above, claim 8 patentably distinguishes over the cited prior art, and the rejection of claim 8 under 35 U.S.C. §103(a) should be withdrawn. Accordingly, claim 8 is in allowable condition.

Because claims 9-14 depend from and further limit claim 8, claims 9-14 are in allowable condition for at least the same reasons.

Claims 15-21

Claim 15 is directed to a memory circuit board for a data storage system. The memory circuit board includes (a) an input/output port to connect with a processor circuit board of the data storage system; (b) a set of memory locations, at least some of the memory locations forming a cache that temporarily stores copies of data elements stored in a set of storage devices of the data storage system; and (c) a controller coupled to the input/output port and the set of memory locations. The controller is configured to (i) receive, from the processor circuit board through the input/output port, a communication that includes a script command and a payload, the payload including a series of individual instructions, (ii) parse the payload to identify the series of individual instructions in response to the script command, and (iii) perform a series of operations in accordance with the identified series of individual instructions.

As mentioned above in connection with claim 8, the cited prior art does not teach or suggest, either alone or in combination, a memory circuit board configured to (i) receive, from the processor circuit board, a communication that includes a script command and a payload, the payload including a series of

individual instructions, (ii) parse the payload to identify the series of individual instructions in response to the script command, and (iii) perform a series of operations in accordance with the identified series of individual instructions. Accordingly, claim 15 patentably distinguishes over the cited prior art for at least the same reasons as claim 8. Thus, the rejection of claim 15 under 35 U.S.C. §103(a) should be withdrawn, and claim 15 is in allowable condition.

Because claims 16-21 depend from and further limit claim 15, claims 16-21 are in allowable condition for at least the same reasons.

Claim 22

Claim 22 is directed to a processor circuit board for a data storage system. The processor circuit board includes (a) an input/output port to connect with a memory circuit board of the data storage system; and (b) control circuitry coupled to the input/output port. The control circuitry is configured to provide, to the memory circuit board through the input/output port, a communication that includes a script command and a payload. The payload includes a series of individual instructions. The script command is configured to direct the memory circuit board to (i) parse the payload to identify the series of individual instructions in response to the script command, and (ii) perform a series of operations in accordance with the identified series of individual instructions.

As mentioned above in connection with claim 8, the cited prior art does not teach or suggest, either alone or in combination, a processor circuit board configured to communicate with a memory circuit board which (i) receives, from the processor circuit board, a communication that includes a script command and a payload, the payload including a series of individual instructions, (ii) parses the payload to identify the series of individual instructions in response to the script command, and (iii) performs a series of operations in accordance with the identified series of individual instructions. Accordingly, claim 22 patentably distinguishes over the cited prior art for at least the same reasons as claim 8.

Thus, the rejection of claim 22 under 35 U.S.C. §103(a) should be withdrawn, and claim 22 is in allowable condition.

Newly Added Claims

Claims 23-30 have been added and are believed to be in allowable condition. Claims 23-24 depend from claim 1. Claims 25-26 depend from claim 8. Claims 27-28 depend from claim 15. Claims 29-30 depend from claim 22. Support for claims 23-30 is provided within the Specification, for example, on page 7, line 4 through page 8, line 20; page 10, line 15 through page 12, line 2; and Figs. 1 and 4. No new matter has been added.

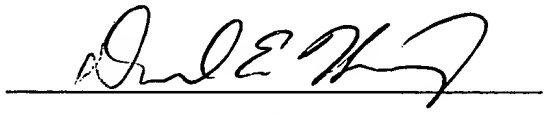
Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Amendment, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicant's Representative at the number below.

Applicant hereby petitions for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this Amendment, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-0901.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 366-9600, in Westborough, Massachusetts.

Respectfully submitted,



David E. Huang, Esq.
Attorney for Applicant(s)
Registration No.: 39,229
CHAPIN & HUANG, L.L.C.
Westborough Office Park
1700 West Park Drive
Westborough, Massachusetts 01581
Telephone: (508) 366-9600
Facsimile: (508) 616-9805

Attorney Docket No.: EMC01-31(01129)

Dated: November 30, 2004